MEG-02-015

November 14, 2005

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/685,872 10/15/03 |
M.S. Lin
POST PASSIVATION INTERCONNECTION SCHEMES ON TOP OF THE IC CHIPS

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on November 14, 2005.

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Stephen B. Ackerman, Reg.# 37761

Signature/Date 11/14/05

The Commissioner is hereby authorized to charge the IDS Processing Fee of $180, under 37 CFR 1.17(p), to Deposit Account No. 19-0033. A duplicate copy of this sheet is enclosed.

U.S. Patent 6,495,442 to Lin et al., "Post Passivation Interconnection Schemes on Top of the IC Chips," discloses a method for the creation of interconnect lines.

U.S. Patent 6,383,916 to Lin, "Top Layers of Metal for High Performance IC's," discloses a method of closely interconnecting integrated circuits contained within a semiconductor wafer to electrical circuits surrounding the semiconductor wafer.

U.S. Patent 6,303,423 to Lin, "Method for Forming High Performance System-On-Chip Using Post Passivation Process," discusses creating high quality electrical components, such as inductors, capacitors or resistors, on a layer of passivation or on the surface of a thick layer of polymer. In addition, the process of the invention provides a method for mounting discrete electrical components at a significant distance removed from the underlying silicon surface.

U.S. Patent 6,649,509 to Lin et al., "Post Passivation Metal Scheme for High-Performance Integrated Circuit Devices," discloses a post-passivation metal interconnect scheme over the surface of an IC device that has been covered with a conventional layer of passivation.

U.S. Patent Application Publication US 2003/0222295 A1 to Lin, "High Performance System-On-Chip Inductor Using Post Passivation Process," describes a system and method for forming post passivation inductors, and related structures.

U.S. Patent 5,659,201 to Wollesen, "High Conductivity Interconnection Line," discloses high conductivity interconnection lines formed of high conductivity material, such as copper, employing barrier layers impervious to the diffusion of copper atoms.

U.S. Patent 6,187,680 to Costrini et al., "Method Structure for Creating Aluminum Wirebound Pad on Copper BEOL," discloses a method for fabricating an integrated circuit (IC) structure having an Al contact in electrical communication with Cu wiring embedded in the initial semiconductor wafer.

U.S. Patent Application Publication US 2002/0158334 A1 to Vu et al., "Microelectronic Device Having Signal Distribution Functionality on an Interfacial Layer Thereof," discloses a microelectronic die having an interfacial metal layer deposited over an active surface thereof to perform a signal destribution function within the device.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
MEG-02-015	10/685,872
Applicant: M.-S. Lin	
Filing Date: 10/15/03	Group Art Unit

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6495442	12/17/02	Lin et al.	438	618	10/18/00
	6383916	5/7/02	Lin	438	637	2/17/99
	6303423	10/16/01	Lin	438	238	11/27/00
	6649509	11/18/03	Lin et al.	438	618	10/24/01
	5659201	8/19/97	Wollesen	257	758	6/5/95
	6187680	2/13/01	Costrini et al.	438	688	10/7/98

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

-	U.S. Patent App. Pub. US 2003/0222295 A1 to Lin, Pub. Date 12/4/03, Filed 5/27/03, US Cl. 257/300.
-	U.S. Patent App. Pub. US 2002/0158334 A1 to Vu et al., Pub. Date 10/31/02, Filed 04/30/01, US Cl. 257/723.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.